CLAIMS

1.   An electronic device, comprising:

a memory structure comprising an integer M of word storage locations;

a shift register for storing a sequence of bits, wherein the sequence in the shift register comprises a number of bits equal to a ratio of $1/R_1$ times the integer M; and

5   circuitry for providing a clock cycle to the shift register for selected data operations with respect to any of the word storage locations, wherein the selected data operations are a data read or a data write;

wherein in response to each clock cycle, received from the circuitry for providing the clock cycle, the shift register shifts the sequence; and

10   wherein one bit in the sequence corresponds to an indication of one of the memory word storage locations from which a word will be read or into which a word will be written.

2.   The electronic device of claim 1:

wherein the sequence comprises a first number of bits of a first state;

wherein the sequence comprises a second number of contiguous bits of a second state that is complementary to the first state; and

5   wherein the first number plus the second number equals the ratio of $1/R_1$ times the integer M.

3.   The electronic device of claim 2 wherein the first number of bits includes the one bit in the sequence that corresponds to an indication of one of the memory word storage locations.

4.   The electronic device of claim 3 wherein the first number of bits is less than the second number of contiguous bits.

5.   The electronic device of claim 4 wherein the first number of bits equals one bit.

6.   The electronic device of claim 4 wherein the first number of bits is greater than one bit.

7.   The electronic device of claim 4 wherein the first number of bits equals three bits.

8.   The electronic device of claim 1:

wherein the shift register comprises a write shift register;

wherein the circuitry for providing is for providing a write clock cycle to the write shift register for selected write data operations with respect to any of the word storage locations;

wherein in response to each write clock cycle, received from the circuitry for providing the write clock cycle, the write shift register shifts the sequence in the write register;

wherein one bit in the sequence in the write register corresponds to an indication of one of the memory word storage locations into which a word will be written;

and further comprising a read shift register for storing a sequence of bits, wherein the sequence stored in the shift register comprises a number of bits equal to a ratio of $1/R_2$ times the integer M;

wherein the circuitry for providing is further for providing a read clock cycle to the read shift register for selected read data operations with respect to any of the word storage locations;

wherein in response to each read clock cycle, received from the circuitry for providing the read clock cycle, the read shift register shifts the sequence in the read register; and

wherein one bit in the sequence in the read shift register corresponds to an indication of one of the memory word storage locations from which a word will be read.

9.   The electronic device of claim 8 and further comprising circuitry for detecting a collision with respect to one location of the word storage locations, wherein the collision comprises either a potential write of data over unread data in the one location or a potential read of invalid data in the one location.

10.   The electronic device of claim 9 wherein the circuitry for detecting a collision comprises a single logic stage having a first input coupled to the read shift register and a second input coupled to the write shift register.

11.   The electronic device of claim 10 wherein the first input is coupled to a single bit location in the read shift register and the second input is coupled to a single like-positioned bit location in the write shift register.

12.   The electronic device of claim 11 wherein the circuitry for detecting a collision comprises an AND gate.

13.   The electronic device of claim 10 wherein each of the write shift register and the read shift register comprises a wraparound shift register.

14.   The electronic device of claim 10 and further comprising, responsive to the circuitry for detecting a collision, circuitry for resetting a sequence of bits in the read shift register and for resetting a sequence of bits in the write shift register.

15.   The electronic device of claim 14 wherein the reset sequence of bits in the read shift register is offset from the reset sequence of bits in the write shift register by a distance of the integer M divided by two.

16.   The electronic device of claim 9 wherein the circuitry for detecting comprises, for each bit location in the write shift register and for a respective bit location in the read shift register, a single logic stage having a first input coupled to the bit location in the write shift register and a second input coupled to the respective bit location in the read shift register.

17.   The electronic device of claim 8 wherein each of the write shift register and the read shift register comprises a wraparound shift register.

18.   The electronic device of claim 8:

wherein the sequence in the read shift register comprises a first number of bits of a first state;

wherein the sequence in the read shift register comprises a second number of contiguous bits of a second state that is complementary to the first state in the read shift register; and

wherein the first number in the read shift register plus the second number in the read shift register equals the ratio of $1/R_2$ times the integer M.

19.   The electronic device of claim 18 wherein the first number of bits in the read shift register includes the one bit in the sequence in the read shift register that corresponds to an indication of one of the memory word storage locations.

20.   The electronic device of claim 19 wherein the first number of bits in the read shift register is less than the second number of contiguous bits in the read shift register.

21.   The electronic device of claim 20 wherein the first number of bits in the read shift register equals one bit.

22.   The electronic device of claim 20 wherein the first number of bits in the read shift register is greater than one bit.

23.   The electronic device of claim 20 wherein the first number of bits in the read shift register equals three bits.

.24.   The electronic device of claim 8:

wherein the sequence in the write shift register comprises a first number of bits of a first state;

wherein the sequence in the write shift register comprises a second number of
5   contiguous bits of a second state that is complementary to the first state in the write shift register; and

wherein the first number in the write shift register plus the second number in the write shift register equals the integer $1/R_1$ times the integer M.

25.   The electronic device of claim 8 wherein R_1 equals R_2.

26.   The electronic device of claim 8 wherein R_1 and R_2 both equal one.

27.   The electronic device of claim 8:

wherein the circuitry for providing a write clock cycle to the write shift register for selected write data operations provides a write clock cycle for every R_1 write data operations with respect to any of the word storage locations; and
5   wherein the circuitry for providing a read clock cycle to the read shift register for selected read data operations provides a read clock cycle for every R_2 read data operations with respect to any of the word storage locations.

28. A method of operating an electronic device, the electronic device comprising a memory structure comprising an integer M of word storage locations, the method comprising:

providing a plurality of clock cycles;

5   for each clock cycle in the plurality of clock cycles, performing a data operation with respect to any of the word storage locations, wherein the data operation is a data read or a data write;

for selected ones of the clock cycles, shifting a sequence bits, the sequence of bits comprising a number of bits equal to a ratio of $1/R_1$ times the integer M;

10   wherein one bit in the sequence corresponds to an indication of one of the word storage locations from which a word will be read or into which a word will be written.

29. The method of claim 28:

wherein the sequence comprises a first number of bits of a first state;

wherein the sequence comprises a second number of contiguous bits of a second state that is complementary to the first state; and

5   wherein the first number plus the second number equals the ratio of $1/R_1$ times the integer M.

30. The method of claim 29 wherein the first number of bits includes the one bit in the sequence that corresponds to an indication of one of the memory word storage locations.

31. The method of claim 30 wherein the first number of bits is less than the second number of contiguous bits.

32.   The method of 28:

wherein the providing step is for providing a plurality of write clock cycles;

wherein the step of performing a data operation comprises, for each write clock cycle in the plurality of write clock cycles, performing a write data operation with respect to any of the word storage locations;

wherein the step of shifting a sequence comprises, for selected write clock cycles in the plurality of write clock cycles, operating a write shift register to shift the sequence in the write shift register;

wherein one bit in the sequence in the write register corresponds to an indication of one of the memory word storage locations into which a word will be written;

and further comprising:

providing a plurality of read clock cycles;

for each read clock cycle in the plurality of read clock cycles, performing a read data operation with respect to any of the word storage locations;

for selected ones of the read clock cycles, shifting a sequence of bits in a read shift register, the sequence of bits in the read shift register comprising a number of bit equal to a ratio of $1/R_2$ times the integer M;

wherein one bit in the sequence in the read shift register corresponds to an indication of one of the memory word storage locations from which a word will be read.

33.   The method of claim 32 and further comprising detecting a collision with respect to one location of the word storage locations, wherein the collision comprises either a potential write of data over unread data in the one location or a potential read of invalid data in the one location.

34.   The method of claim 33 wherein the step of detecting a collision comprises operating a single logic stage having a first input coupled to the read shift register and a second input coupled to the write shift register.

35.   The method of claim 32 wherein R_1 equals R_2.

36.   The method of claim 32 wherein R_1 and R_2 both equal one.

37.   The method of claim 32:

wherein the step of operating a write shift register for selected write clock cycles comprise operating the write shift register for every R_1 write clock cycles; and

wherein the step of operating a read shift register for selected read clock cycles comprise operating the read shift register for every R_2 read clock cycles.

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